A LOW-NOISE L-BAND DIELECTRIC RESONATOR STABILIZED MICROSTRIP OSCILLATOR

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ABSTRACT

Design and performance of a unique microstrip L-band bipolar transistor dielectric resonator stabilized oscillator (DRO) is described which achieves ultralow single-sideband phase noise (−163 dBc/Hz at 100 kHz offset frequency), low 1/f noise corner frequency of 12 kHz, with near-constant frequency (1280 ± 0.06 MHz) and power (12.55 ± 0.15 dBm) over −50° to 75°C Circuit details to minimize noise as well as transistor selection criteria and measurements are presented. Back-to-back varactors provide 350 kHz electronic tuning range for phase-locking applications without any increase of noise.

INTRODUCTION

Low phase noise oscillators with constant frequency and power over temperature is required in new emerging systems for improved spectral purity, lower cost, and simplicity. A fixed tuned stable oscillator with these desirable features and low 1/f noise is a key element in modern stable local oscillators. This source with an electronic tuning port can be used in conjunction with a crystal multiplier source in an active phased-locked filter to reduce crystal multiplier noise by as much as 20 dB. It can also be used as a primary source due to the accurate frequency characteristics.

Silicon bipolar transistors were investigated over GaAs FET devices due to their inherent lower near-carrier noise capability (1, 2, 3). The best known reported FET oscillator noise by Lan et al. (4) is still some 3 to 7 dB higher than this work when scaled to the same frequency. Recent results by Agarwal (5) using the GaAs/(Ga,Al)As heterojunction bipolar transistor indicate near-carrier noise between the silicon bipolar and the GaAs FET. Very little published information could be found concerning the noise behavior of commercially available bipolar transistors, which is reported in this work.

This paper will first report on noise measurements made at baseband for many bipolar transistors to select candidate transistors for the oscillator. Circuit details will next be presented on the transistor feedback circuit as well as circuits to minimize the upconversion of this baseband noise to RF for a low 1/f noise corner frequency. Dielectric resonator measurements, including circuit Q, the effect of metallic walls, and frequency-temperature sensitivity, will be presented for many resonators. The coupling techniques between the transistor, resonator, tuning varactors, and load will next be described. Bias circuits as well as the integrated buffer amplifier details for low noise and stability will be presented. Finally, the oscillator performance over temperature and tuning voltage will be presented.

BASEBAND NOISE MEASUREMENTS

To select candidate transistors to be used in the oscillator, equivalent baseband current and voltage noise as well as h_{fe} as a function of collector current were measured for many bipolar transistors. The baseband noise was examined because this noise is upconverted to the RF carrier in the nonlinear oscillator process. Transistors that have low noise values coupled with low upconversion of baseband noise will result in a low near-carrier phase noise oscillator. The transistors should have low noise figures at the values of current at which they are being operated. A transistor with low noise figure at low current values and small-signal-handling capacity will not have the lowest oscillator phase noise. Transistors with moderate noise figure at higher current values with linear high current capacity generally make good low-noise oscillators. Finally, a transistor with a high h_{fe} and an h_{fe} that does not degrade with low values of collector current is a good indicator of low base recombination, the latter being a cause for bipolar transistor 1/f noise (6).

A Quan-Tech Laboratories, Inc., Model 310 Transistor Noise Analyzer was used to perform the noise and h_{fe} measurements. The noise parameters were for the common-emitter configuration and were referred to the base-to-emitter terminals. The noise measurements were made at 100 Hz, 1 kHz, and 10 kHz to examine the 1/f noise characteristics.

The results for eight transistors are presented in tables 1 through 4.

Table 1. Transistor Baseband Noise; HP3102 and HP3104

Transistor	I_C (mA)	h_{fe}	Voltage Noise (Nanovolts/√Hz)			Current Noise (Picoamps/√Hz)		
			100 Hz	1 kHz	10 kHz	100 Hz	1 kHz	10 kHz
HP 3102	0.2	15	84	3.6	2.0	70	21	5.6
	0.3	18	68	2 9	1.6	100	30	8.0
	1	20	45	1 8	1 0	160	42	1.6
	3	22	28	1 6	0.9	190	64	25.0
	5	24	29	2.0	1 1	270	82	34.0
	10	29	30	2 4	1.2	-	110	44.0
	20	40						
	Low h_{fe}		Moderate Voltage Noise			High Current Noise		
HP 3104	0.2	9	33	3 4	1 6	74	16	7
	0.3	9	26	2.5	1.3	70	18	8
	1	9	16	1.7	0 9	190	32	10
	3	10	Oscillation			>300	70	17
	5	10	2200	800	3	>300	76	18
	10	15	3000	1900	70	>300	110	29
	Low h_{fe}		High Voltage Noise			High Current Noise		

Table 2. Transistor Baseband Noise; NEC645 and Motorola 2N5943

Transistor	I_C (mA)	h_{fe}	Voltage Noise (Nanovolts/√Hz)			Current Noise (Picoamps/√Hz)		
			100 Hz	1 kHz	10 kHz	100 Hz	1 kHz	10 kHz
NEC 645	0 2	79	190	6	2.0	300	90	30
	0.3	83	150	4 2	1.6	-	95	35
	0 5	91	130	3.4	1 2	-	110	42
	1	98	120	2 6	1.0	-	-	60
	2	102	42	1 6	0 9	-	-	Oscillation
	3	102	39	1.6	0 9	-	140	170
V_{CE} = 8 V	5	102	58	3.3	1.3	-	120	82
	10	105	65	4.0	1.4	-	-	Oscillation
	20	95	60	4 6	1.7	-	100	21
	Excellent h_{fe}		Moderate Voltage Noise			High Current Noise		
Motorola 2N5943	0.2	58	58	2.2	1 6	9.5	15	15
	0 3	58	54	1 9	1.3	8.8	17	17
	1	59	36	1 3	0.8	8 8	2.6	2.4
	3	60	21	1 0	0.7	15.0	4.4	3.8
	5	60	25	1 1	0.8	17 0	5.6	4.6
	10	61	20	1 0	0.8	26.0	8 0	6 4
	20	70	19	1 3	1.0	32.0	11	8 6
	30	70	40	2 0	1.1	44 0	14	9.6
	Moderate h_{fe}		Moderate Voltage Noise			Low Current Noise		

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Table 3. Transistor Baseband Noise; NEC221 and NEC773

Transistor	I_C (mA)	h_{fe}	Voltage Noise (Nanovolts/$\sqrt{Hz}$) 100 Hz	1 kHz	10 kHz	Current Noise (Picoamps/$\sqrt{Hz}$) 100 Hz	1 kHz	10 kHz
NEC 221	0.2	33	180	4.4	2.4	22	1.8	1.2
V_{CE} = 10 V	0.3	40	130	3.0	1.8	28	2.8	1.8
	1	55	70	2 8	0 9	9	5.8	2.9
	2	60	54	1 5	0 7	42	8.5	4.2
	3	65	65	1.6	0 7	48	10.0	5.0
	5	68	44	1.4	0.8	54	14.0	6.2
	10	76	41	1.4	0.8	750	20.0	8.8
	20	79	30	1.8	1.0	130	28.0	12.0
	30	80	45	2.3	1.2	170	34.0	14.0
Moderate h_{fe}			Moderate Voltage Noise			High Current Noise		
NEC 773	0 2	25	140	4.0	1.8	25	2.3	1.5
	0 3	25	140	3.0	1.4	30	3.0	2.0
	1	30	56	1 7	0.8	27	5.7	3.4
	2	35	58	1.8	0.7	42	8.0	4.5
	3	35	55	1.4	0.7	48	10.0	5.5
	5	38	54	1.6	0.7	50	12.0	6.4
	10	40	53	1.4	0.7	70	18.0	9.4
	20	42	52	1.6	1.0	80	24 0	12.0
	30	43	50	2.0	1.2	150	30.0	14.0
Low h_{fe}			Moderate Voltage Noise			High Current Noise		

Table 4. Transistor Baseband Noise; NEC416 and NEC595

Transistor	I_C (mA)	h_{fe}	Voltage Noise (Nanovolts/$\sqrt{Hz}$) 100 Hz	1 kHz	10 kHz	Current Noise (Picoamps/$\sqrt{Hz}$) 100 Hz	1 kHz	10 kHz
NEC 416	0 1	67	50	4.4	2	21	1.7	1.4
V_{CE} = 10 V	0 3	75	70	2 1	1.3	15	2.5	1.7
	1	88	50	1.6	0 8	20	4.5	2.5
	3	95	23	1.1	0.6	40	8.5	4.0
	10	103	28	1.2	0 8	80	20.0	7.0
	30	118	14	1.9	1.1	50	12 0	4.0
High h_{fe}			Lowest Voltage Noise			Lowest Current Noise		
	0 2	85	31	3.1	1.6	5.4	1.7	1.5
NEC 595	0.3	89	26	1 5	1.3	5 0	1.7	1.5
V_{CE} = 10 V	1	92	15	1.5	0.8	6.0	2.4	2.2
	2	92	13	1.2	0.7	9.0	3.2	2.8
	3	92	12	1.2	0.7	12.0	4.0	3.4
	5	90	12	1.2	0.7	15.0	5.2	4.2
	10	89	11	1.2	0.7	28.0	8.0	5.8
	20	88	12	1.6	0.8	33.0	12.0	7.4
	30	88	14	2.2	1.0	44.0	15.0	8.8
High h_{fe}			Lowest Voltage Noise			Lowest Current Noise		

Of all the transistors, the NEC NE416 and NE595 exhibited the best overall performance, namely high h_{fe}, low current noise, low voltage noise, and high h_{fe} that does not degrade with low values of collector current. Figure 1 illustrates h_{fe} for various transistors. The NE595 has a near-constant h_{fe} value of 90, while the NE416 has a somewhat higher value at 30 mA collector current, namely 118, that decreases to 67 at 0.1 mA. Figures 2 and 3 illustrate the voltage and current noise respectively for three transistors of the lowest noise. Again, the two cited transistors exhibit the lowest noise. The voltage is about 0.9 nanovolt/$\sqrt{Hz}$ while the current noise is about 7 picoamps/$\sqrt{Hz}$ at 10 kHz for the two transistors. The two transistors were evaluated in the oscillator design.

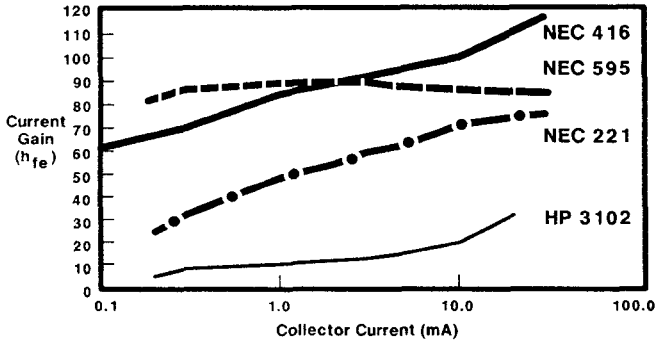


Figure 1. Bipolar Transistor Current Gain Versus Collector Current

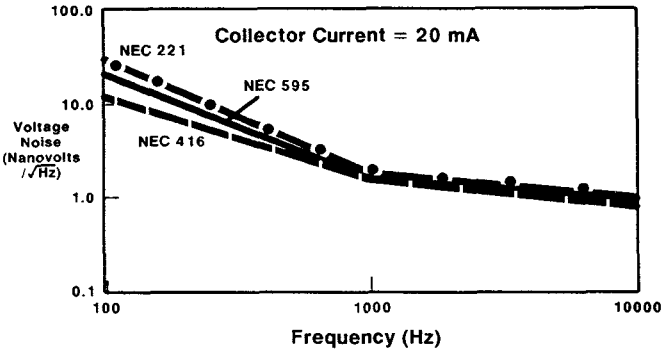


Figure 2. Bipolar Transistor Baseband Voltage Noise Versus Frequency

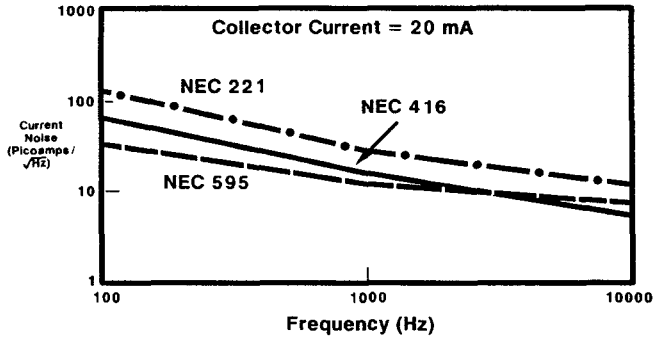


Figure 3. Bipolar Transistor Baseband Current Noise Versus Frequency

OSCILLATOR CIRCUIT

Figure 4 illustrates the schematic of the dielectric resonator stabilized oscillator (DRO), including the oscillator with feedback circuit, the varactor tuning circuit, the resonator network, and the output buffer amplifier. The active oscillator transistor Q1 is in the common-collector configuration with the emitter connected to the feedback capacitor C1 and the base connected to the output power circuit. The value of the emitter feedback capacitance (2.2 pF) was selected so that the reflection coefficient at the base was maximized at the 1.28 GHz center frequency and was greater than 1.

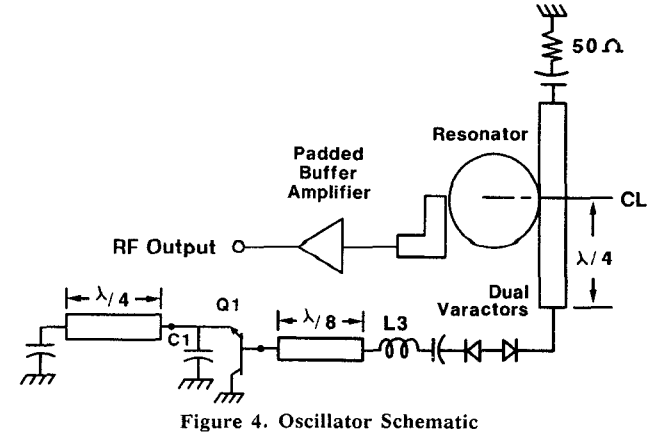


Figure 4. Oscillator Schematic

A noise reduction circuit is also connected to the emitter, which narrows the band where the input reflection coefficient at the base is greater than 1. This circuit prevents noise from being amplified at harmonics and subharmonics of the fundamental. The amplified harmonic noise could then be folded back to the fundamental band in the nonlinear oscillator process and increase the oscillator noise. This circuit consists of a 25-ohm quarter-wavelength line connected to ground through a low-reactance capacitor (47 pF). A 50-ohm resistor connected in series with the base bias circuit also lowers the out-of-band reflection coefficient without affecting the in-band value. Both the base and emitter bias circuits are bypassed with three capacitors (47 pF, 1500 pF, and 22 μF) to provide a low impedance from the kilohertz to gigahertz range.

Back-to-back varactors biased in parallel but in series at RF are located at a low-impedance point of the baseline (one-eighth wavelength from transistor) for maximum varactor tuning range and low power variation with bias voltage. The back-to-back diodes reduce the rectification process and generation of even-order diode harmonics, both of which give rise to noise. The inductor L3 in this implementation is located between the transistor and varactors to resonate the reactance of the varactors.

Dielectric material from Murata and Thompson were evaluated for use in this oscillator. Figure 5 illustrates the measured Q of dielectric resonators at about 1200 MHz for the Murata and Thompson resonators in a large circulator cavity. The effect of moving the lid close to the resonators' top was investigated. With the lid far removed, the Q values were 23,000 and 16,000 for the Murata and Thompson material respectively. The Q values dropped to about 6000 with the lid close to the resonator top.

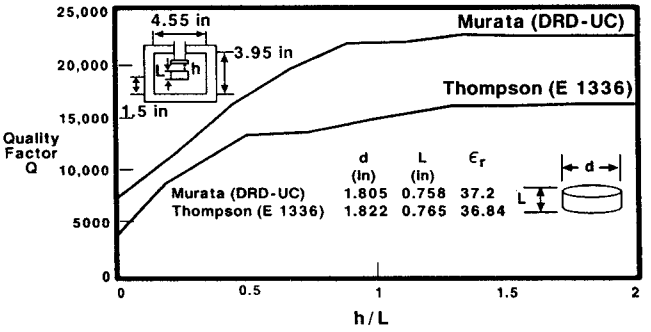
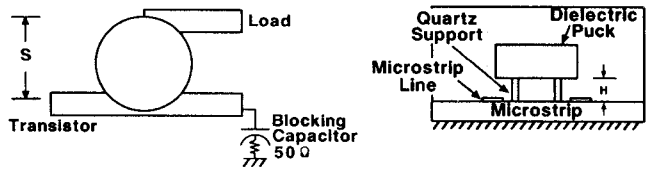


Figure 5. Quality Factor Q of Dielectric Resonators

A transmission cavity as shown in figure 6 was chosen for low-noise considerations. The dielectric resonator was raised above the 0.031-inch-thick 5880 Duroid microstrip with a quartz support for Q considerations. This height (H) as well as the spacing (S) between the coupled microstrip conductors was adjusted simultaneously for 9 dB loss through the filter structure to achieve high external Q and for an input reflection coefficient of 0.64 for optimum output power from the transistor. Figure 7 illustrates the resonator input impedance as well as the configuration details for these requirements. The measured Q was 9365 with all loads connected for the Thompson material. The length of line between the centerline of the resonator and the low impedance of the circuit where the varactors are located is 90 degrees to obtain low-noise stable operation.



H and S Adjusted for ~9 dB Loss Through Filter for High Loaded and External Q. Γ of 0.64 Required for Transistor To Achieve Good Power.

Figure 6. Transmission Cavity

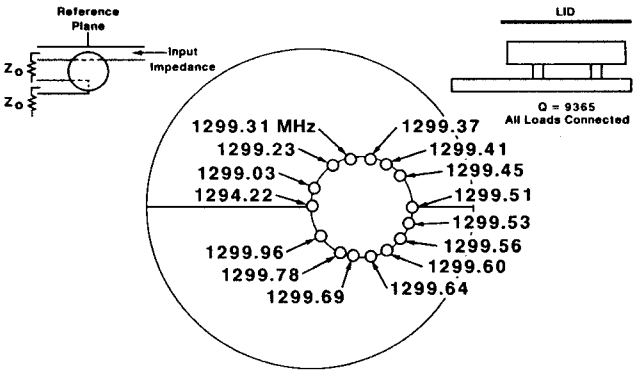


Figure 7. Resonator Input Impedance

The output signal is coupled to a common-emitter buffer amplifier for increased power and isolation from external load changes. A 2-dB pad whose values were selected for unconditional amplifier stability precedes the amplifier while a 3-dB pad precedes the amplifier for increased stability to load changes.

Figure 8 illustrates the completed DRO with the lids removed.

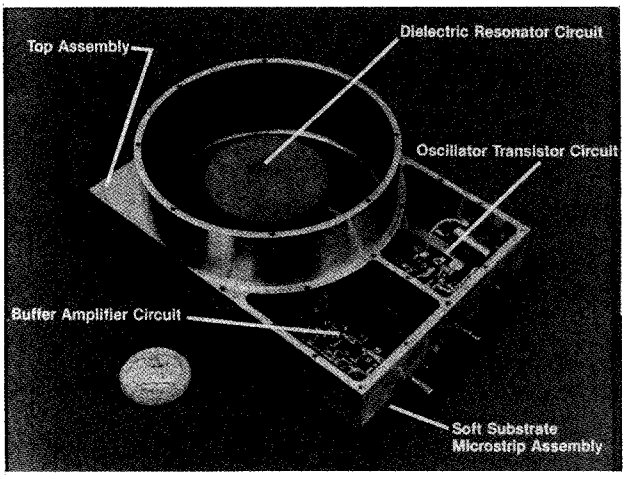


Figure 8. DRO With Lids Removed

EXPERIMENTAL RESULTS

Figure 9 depicts the measured phase noise of the L-band oscillator using the NEC416 device and the Murata resonator. The NE416 exhibited lower noise compared to the NE595 and was operated at 17 mA collector current. The phase noise was experimentally determined to be the lowest at this current value. The phase noise at 100 kHz from the carrier is −163 dBc/Hz and the 1/f noise corner is 12 kHz. This noise is independent of the varactor voltage. A higher Q and an associated lower phase noise could have been achieved if there had been more space available between the microstrip ground and the resonator top lid.

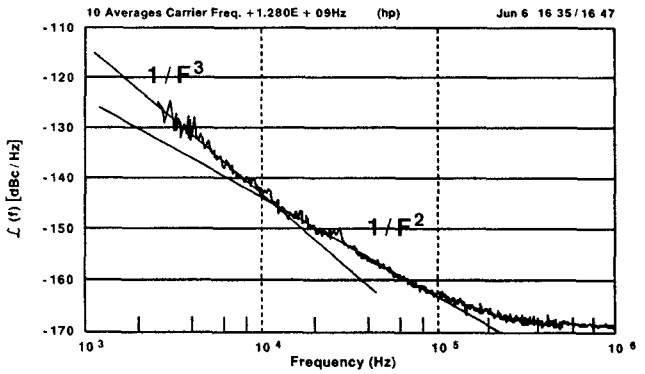


Figure 9. DRO Phase Noise

Figure 10 illustrates the DRO varactor tuning characteristics for two units. Electronic tuning of 350 MHz was obtained with only 1 dB of power variation. Figure 11 depicts the frequency and power versus temperature. The power and frequency variation for a −50° to +75°C temperature excursion was very low: 115 kHz and 0.3 dB respectively.

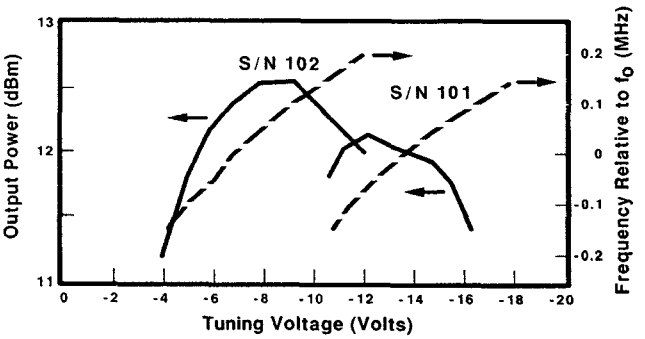


Figure 10. DRO Varactor Tuning Characteristics

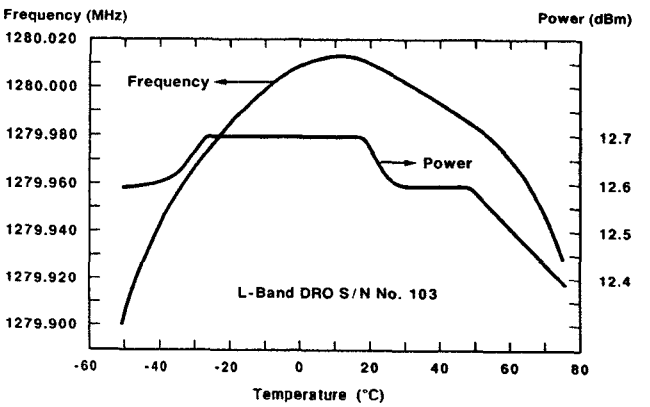


Figure 11. DRO Frequency and Power Versus Temperature

CONCLUSION

A novel microstrip L-band DRO has been realized that provides ultralow phase noise, low 1/f noise corner, near-constant power and frequency over temperature, with a varactor port for phase locking and slight frequency correction. All these desirable parameters have been simultaneously achieved with this circuit.

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